In the Claims:

Claim 1 (currently amended): A method for fabricating a Silicon Based Package (SBP) comprising the steps of:

starting with a wafer composed of silicon and having a first surface and an initial reverse surface which are substantially planar as the base for the SBP;

forming a first interconnection structure over the first surface;

then forming a protective overcoat layer over the interconnection structure;

forming a temporary bond between the protective overcoat layer of the SBP and a wafer holder, with the wafer holder being a rigid structure;

thinning the wafer to a desired thickness to form an Ultra Thin Silicon Wafer (UTSW) for the SBP;

forming Vertical Sidewall Through Via (VSTV) holes which extend through the UTSW with the VSTV holes having bases and substantially vertical sidewalls; ~~and~~

forming metallization in the VSTV holes with the metallization extending through the UTSW; and

bonding the metallization in the VSTV holes to pads of a carrier.

Claims 2 - 13 (canceled).

Claim 14 (amended): A method for fabricating a Silicon Based Package (SBP) comprising the steps of:

providing a base for the SBP comprising a wafer composed of silicon and having a first surface and a reverse surface which are substantially planar;

then forming metal capture structures over the first surface;

then forming a temporary bond between the wafer and a wafer holder, with the wafer holder being a rigid structure leaving the reverse surface of the wafer exposed;

then thinning the reverse surface of the wafer to a desired thickness to form an Ultra Thin Silicon Wafer (UTSW) for the SBP with a thinned reverse surface of the wafer;

then forming Vertical Sidewall Through Via (VSTV) holes with sidewall surfaces and bases which extend from the thinned reverse surface through the wafer with each VSTV hole extending to a surface of the metal capture structures;

then forming a dielectric layer covering the ~~first~~ reverse surface of the silicon wafer including the sidewall surfaces and bases of the VSTV holes;

then etching the dielectric layer to expose the surface of the metal capture structures at the bases of the VSTV holes;

then forming metal pads in the VSTV holes on exposed surfaces thereof with proximal ends being located at the thinned reverse surface and distal ends of the metal pads being in contact with the metal capture structures at the bases of the VSTV holes; and

then forming solder connectors on the metal pads in the VSTV holes.

Claim 15 (original): The method of claim 14 including the steps of:

forming a patterned dielectric hard mask with a pattern of VSTV openings therethrough over the thinned reverse surface of the wafer; and

forming the VSTV holes by etching through the pattern of VSTV openings through the patterned dielectric VSTV hard mask layer and the thinned reverse surface to form VSTV holes, thereby exposing the surface of the metal capture structures.

Claim 16 (original): The method of claim 14 including the steps of:

forming the temporary bond with polyimide; and

releasing the temporary bond by laser ablation.

Claim 17 (original): The method of claim 16 including the steps of:

forming a patterned dielectric hard mask with a pattern of VSTV openings therethrough over the thinned reverse surface of the wafer; and

forming the VSTV holes by etching through the pattern of VSTV openings through the patterned dielectric VSTV hard mask layer and the thinned reverse surface to form VSTV holes, thereby exposing the surface of the metal capture structures; and

then releasing the temporary bond by laser ablation.

Claim 18 (original): The method of claim 14 including the step of bonding the solder ball connectors on the metal pads in the VSTV hole to pads of a carrier.

Claim 19 (original): The method of claim 14 including the step performed prior to thinning of the wafer of burying metal capture pads in a dielectric layer and forming at least one small diameter capture via between each metal capture pad and the first surface of the wafer.

Claim 20 (canceled).

Claim 21 (new): A method for fabricating a Silicon Based Package (SBP) comprising the steps of:

starting with a wafer composed of silicon and having a first surface and an initial reverse surface which are substantially planar as the base for the SBP;

initially forming metal capture structures over the first surface;

forming a first interconnection structure over the first surface;

then forming a protective overcoat layer over the interconnection structure;

forming a temporary bond between the protective overcoat layer of the SBP and a wafer holder, with the wafer holder being a rigid structure;

thinning the initial reverse surface of the wafer by subtractive processing to a desired thickness to form an Ultra Thin Silicon Wafer (UTSW) with a thinned reverse surface for the SBP;

forming Vertical Sidewall Through Via (VSTV) holes in the thinned reversed surface of the UTSW after thinning the wafer which VSTV holes extend through the UTSW with the VSTV holes having bases and substantially vertical sidewalls which expose said metal capture structures;

then forming a dielectric layer over the thinned reverse surface of the UTSW and the sidewalls and bases of the VSTV holes and the exposed metal capture structures;

then removing the dielectric layer from horizontal surfaces including the exposed metal capture structures;

then forming metal pads comprising a metal layer on the exposed metal capture structures and sidewalls of the VSTV holes;

then forming metal conectors on the metal pads; and

then joining the metal connectors to a carrier body.

Claim 22 (new): The method of claim 21 including the steps of:

forming a dielectric hard mask with a pattern of VSTV openings therethrough over the thinned reverse surface of the wafer; and

forming said VSTV holes through the thinned reverse surface through said dielectric VSTV hard mask layer to form said VSTV holes after thinning the wafer to expose said metal capture structures.